Challenges of the Commercial Xilinx Virtex 7 FPGA

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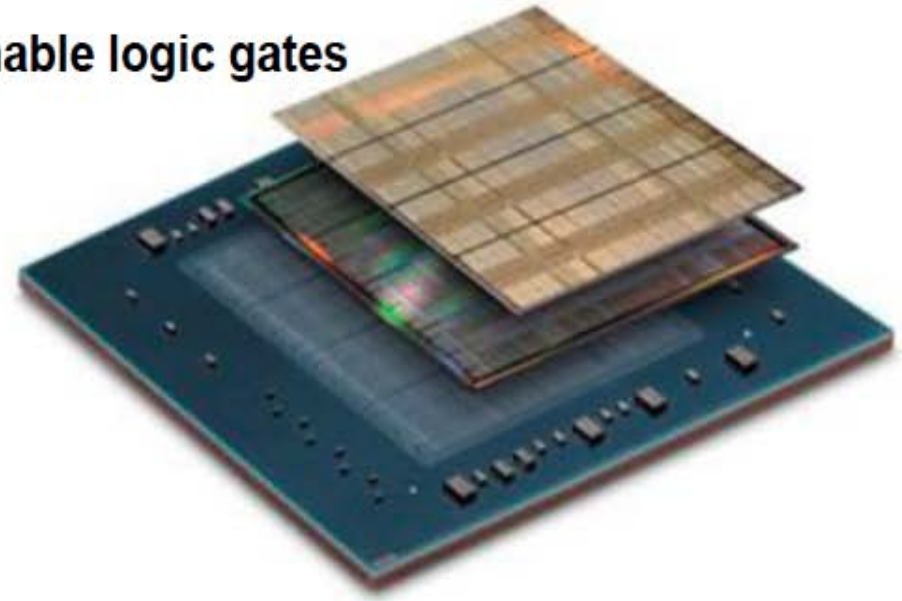
Virtex 7 Overview

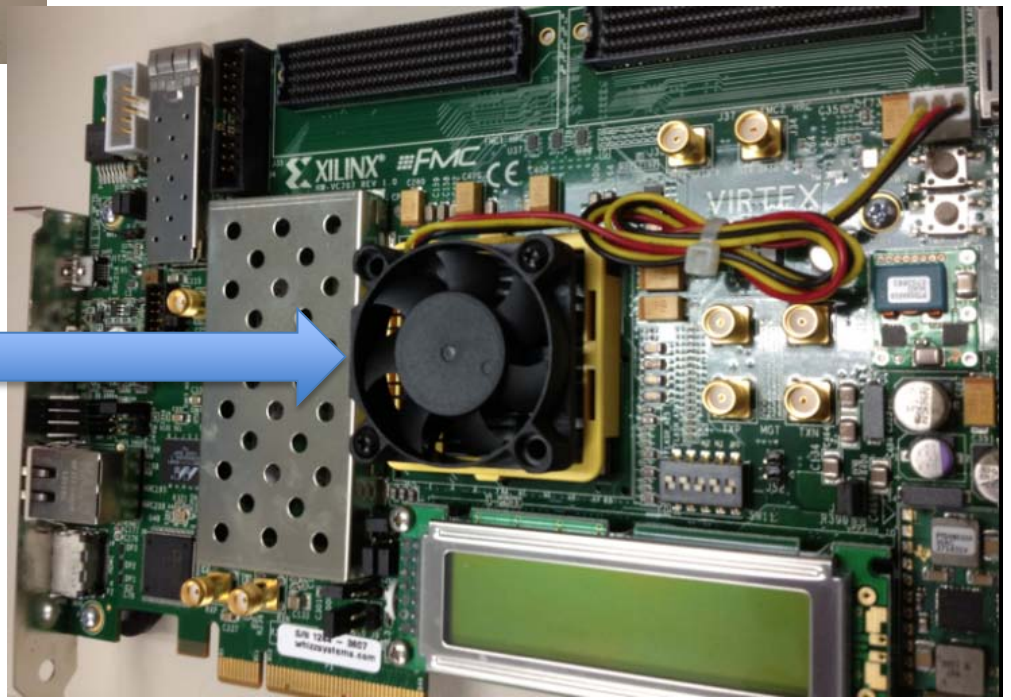
Xilinx Virtex-7 2000T

- **6,800,000,000** transistors
- **1,954,560** logic cells
- **20,000,000** equivalent programmable logic gates
- **1200** user I/Os
- **2.8 Tbps** aggregate bandwidth
- **1.5 Tera MACs**
- **20 Watt**



Virtex 7


XILINX®
VIRTEX®-7
XC7VH580T™
HCG1931ACX1239
AA22092A
KOREA
UNITED STATES OF AMERICA
LIBERTY
QUARTER DOLLAR


XILINX
FMC
VIRTEX

Virtex 7 = 28nm CMOS

28nm process node

- First wave of 28nm HK/MG devices from fabless Si vendors
- >2x device capacity over 40nm devices
- ~50% total power reduction over 40nm devices

Xilinx 28nm High-Performance, Low-Power process

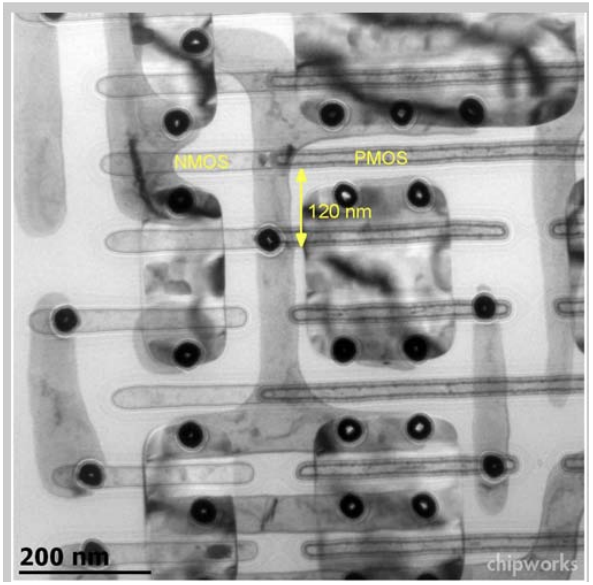
- High-K Metal Gate (HK/MG)
- Developed by Xilinx and TSMC - optimized for high performance & low power
- 65% lower static power than 28nm variants offering similar performance

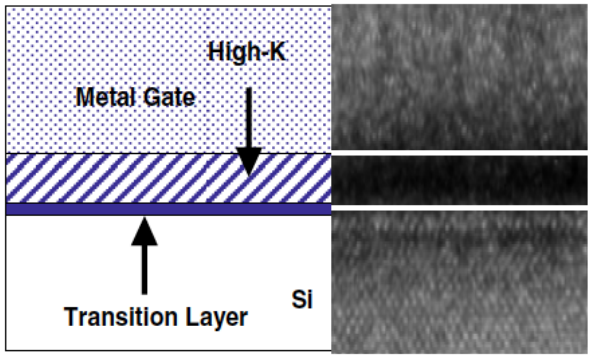
Process	Xilinx 40nm High Performance	28nm Low Power	28nm High Performance	28nm High Performance Low Power
Gate Scheme	SiON/Poly	SiON/Poly	HK/MG	HK/MG
VCC	1V	1.05V	.85V	1V
Static Power	>2.5x	1.5x	2x	1.0x
FPGA Performance*	1.0x	0.9x	1.02x	1.0x

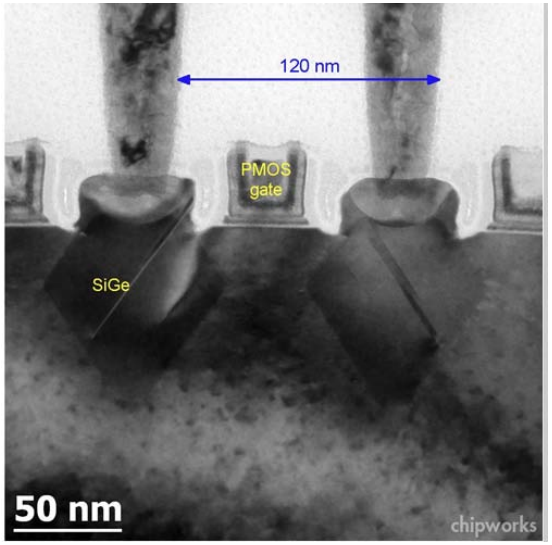
* Estimation of FPGA performance based on Xilinx internal benchmark suite

Challenges – 28nm CMOS

- Metal gate
  - TiN for PMOS
  - TiAlN for NMOS
- High k dielectric gate insulator
  - HfO2 over 2.0nm SiO2
- Process optimizations required but capable of improving of NBTI, SILC, and TDDB ~ 30%

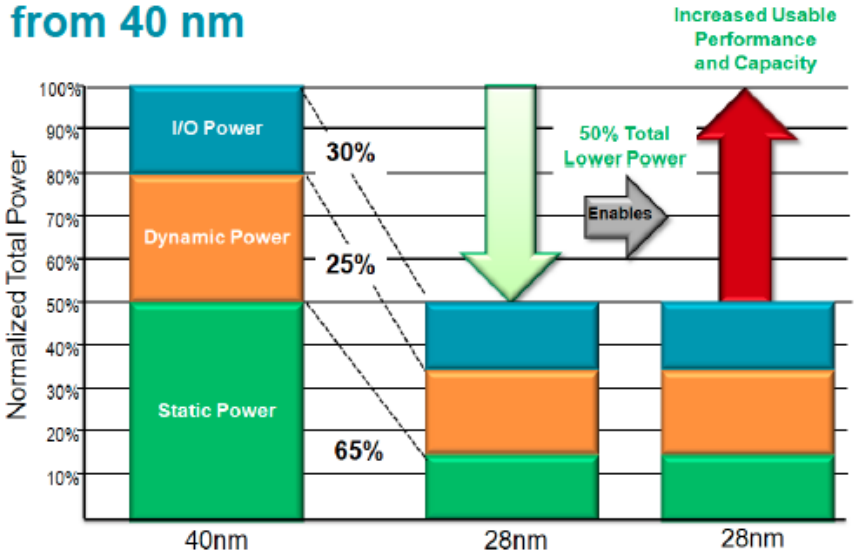




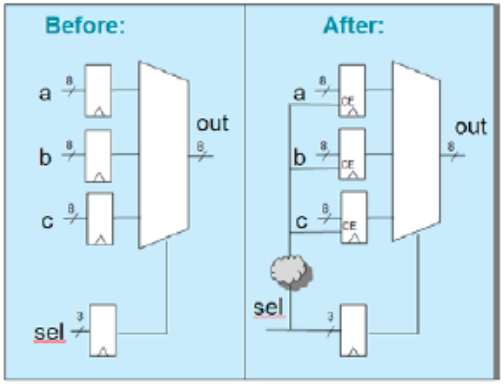


All About Power Reduction

- **New for 28nm – 50% Total Power Reduction from 40 nm**
  - Static Power - 65% reduction
    - Xilinx High Performance Low Power Process
  - Dynamic Power – 25% reduction
    - 40nm => 28nm process shrink
  - IO Power – 30% reduction
    - VCCAUX voltage reduction from 2.5V to 1.8V
    - High Speed Transceiver power saving features
    - Single Ended IO (DDR3) power saving features
    - Support for 1.2V, 1.35V for memory standards



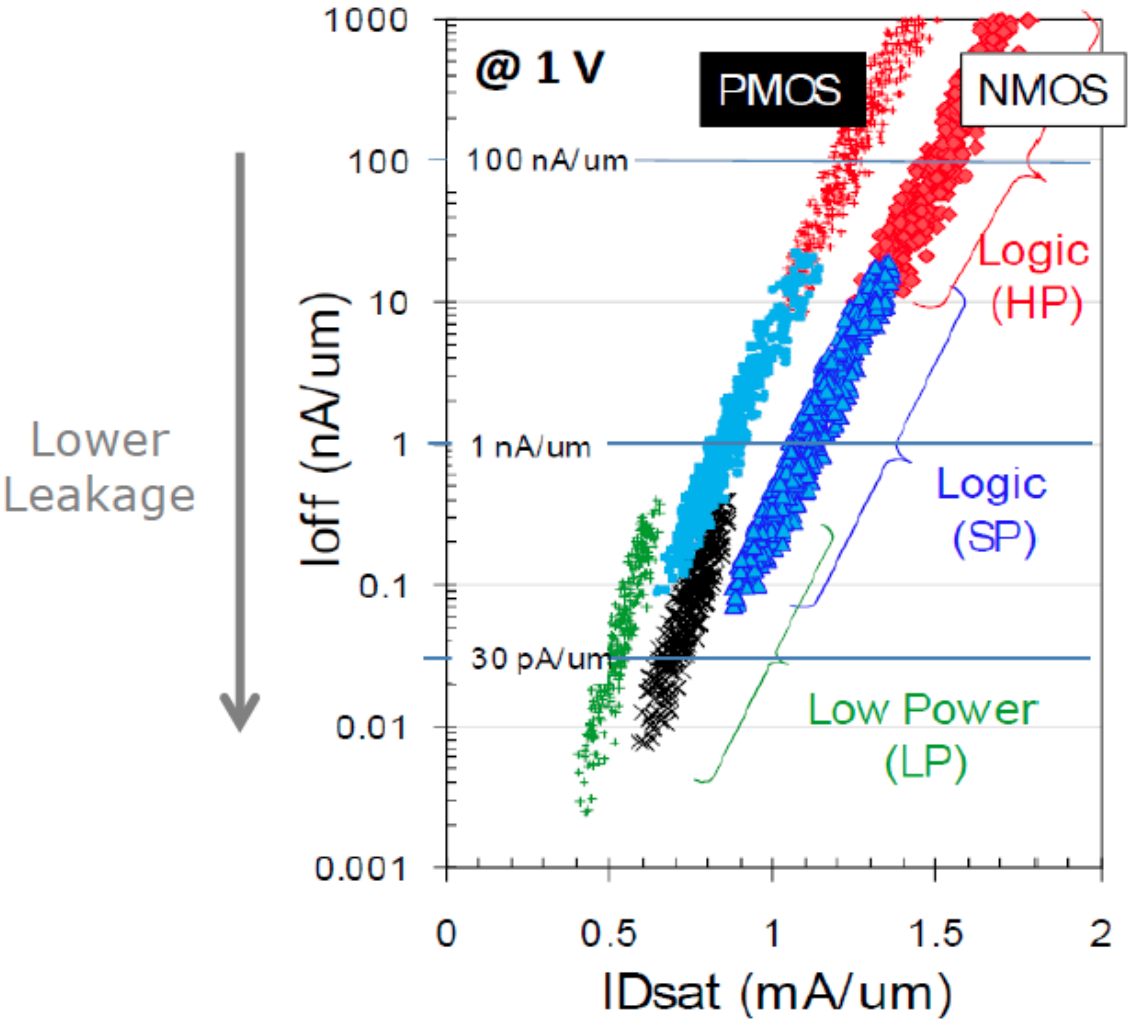
- **Activity Based Logic Optimization – 20% reduction**
  - Available in ISE v12
  - Average 20% savings (benchmark results)
  - Leverages clock gating built into Logic Slice



- **Additional Low Power Device Options**
  - -1L low power .9V speed grades - 20% power reduction

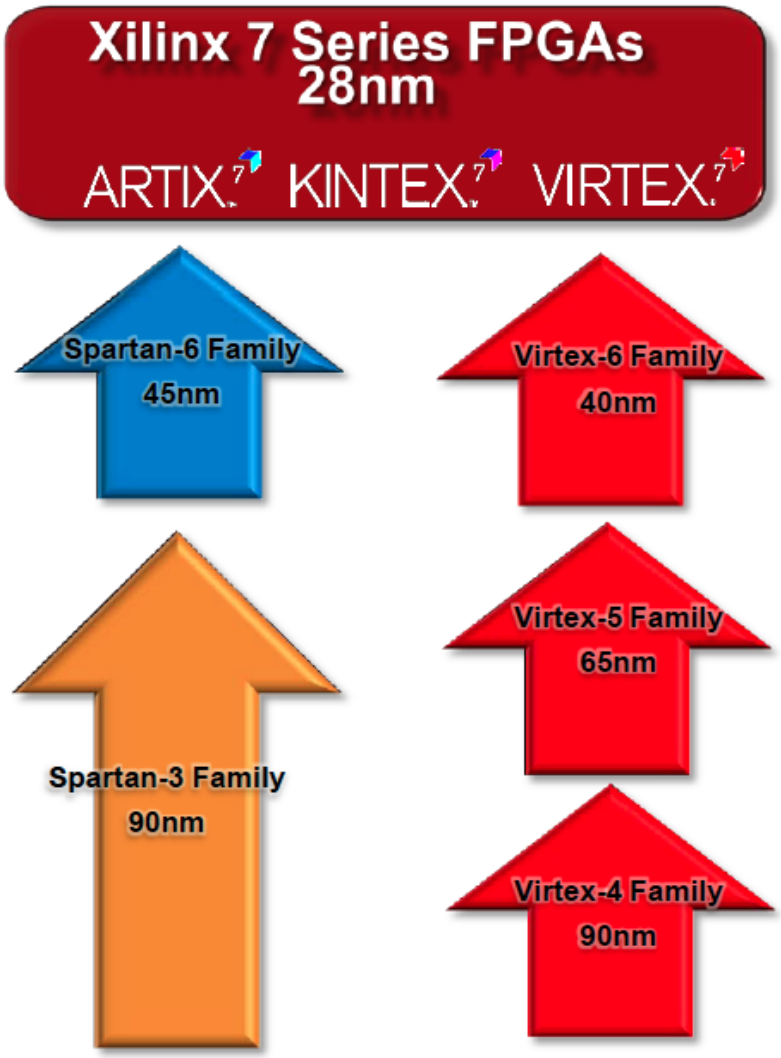
1) Total Power reduction estimated from Xilinx internal benchmarks (Range 45%-61%)
2) Static power reduction for max VCC, 100 DegC, worst case process

Tradeoffs of performance vs. power for various processes



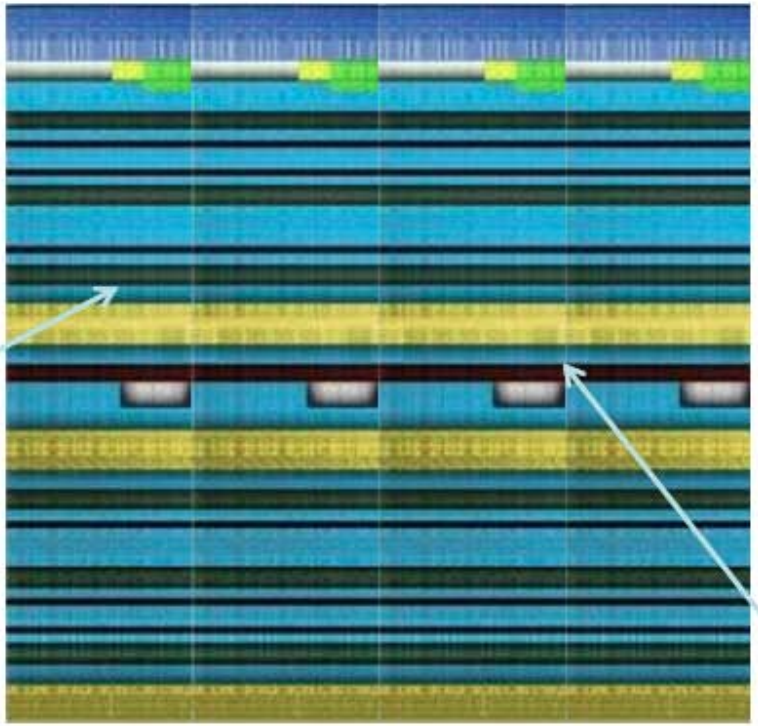
FPGA Architecture Evolution

- **Unified Architecture Advantages**
  - Rapid deployment of 28nm devices
  - Xilinx IP reuse across all devices
  - FPGA tools optimized for Series 7 architecture
  - 3 families for optimal power, cost, performance
- **1st Step Toward Unification**
  - Virtex-6 and Spartan-6 share compatible 6LUT, DSP48 and IO blocks
- **Two FPGA Base Families**
  - Virtex® FPGAs: 4 LUT based high performance, high density family
  - Spartan® FPGAs: 4 LUT based low cost family

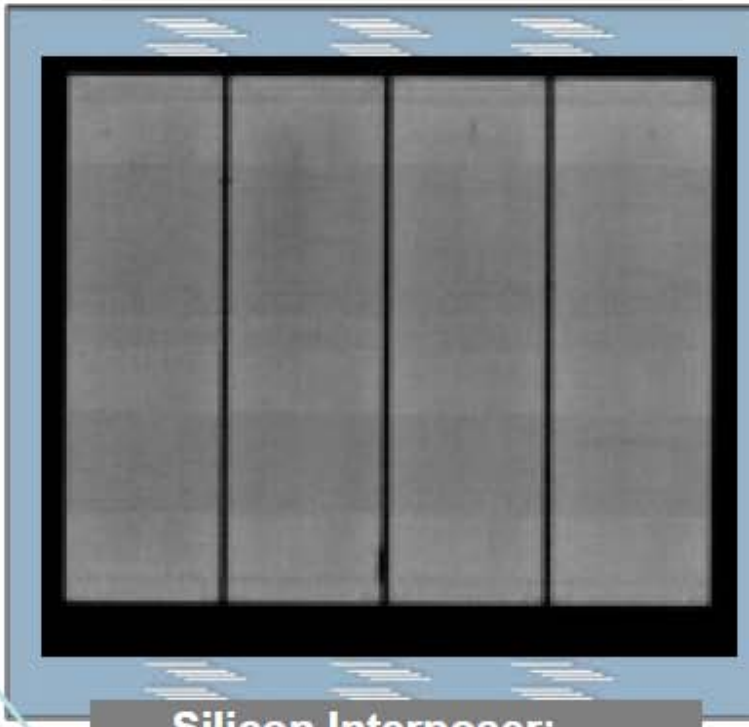


Xilinx 7V2000T FPGA with Stacked Silicon Interconnect Technology

> 6.8B transistors
> 200k microbumps



ASMBL-optimized FPGA slice



FPGA Slices Side-by-Side

Silicon Interposer:

- > 10K routing connections between slices
- ~ 1ns latency

Stacked Silicon Integration

- Xilinx SSI technology is based on Application Specific Modular Block (ASMBL) architecture, a modular structure comprising ‘tile like’ building blocks that implement key functionality:
  - Configurable logic blocks (CLBs), block RAM, DSP slices, SelectIO™ interfaces, and serial transceivers.
- By varying the height and arrangement of columns, an assortment of devices can be created to match different market requirements
- These resources are organized into columns and then combined to create an FPGA.

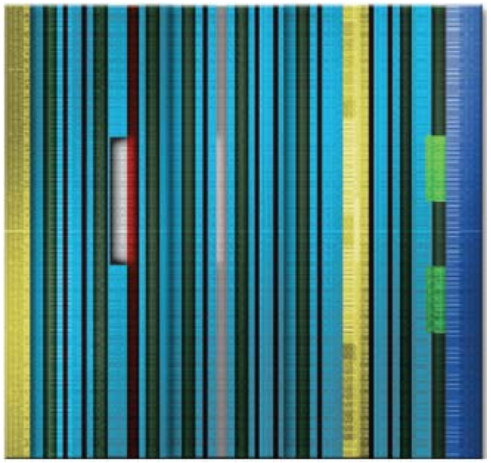
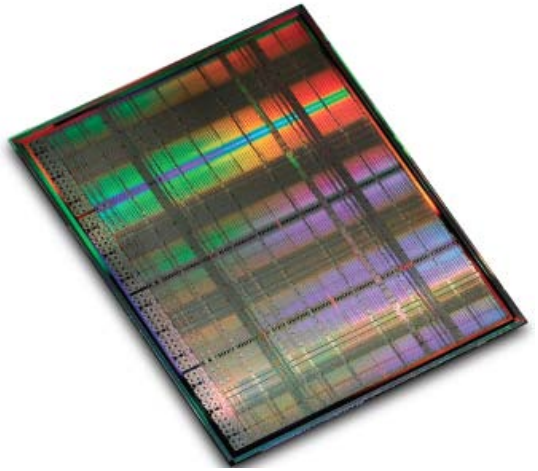


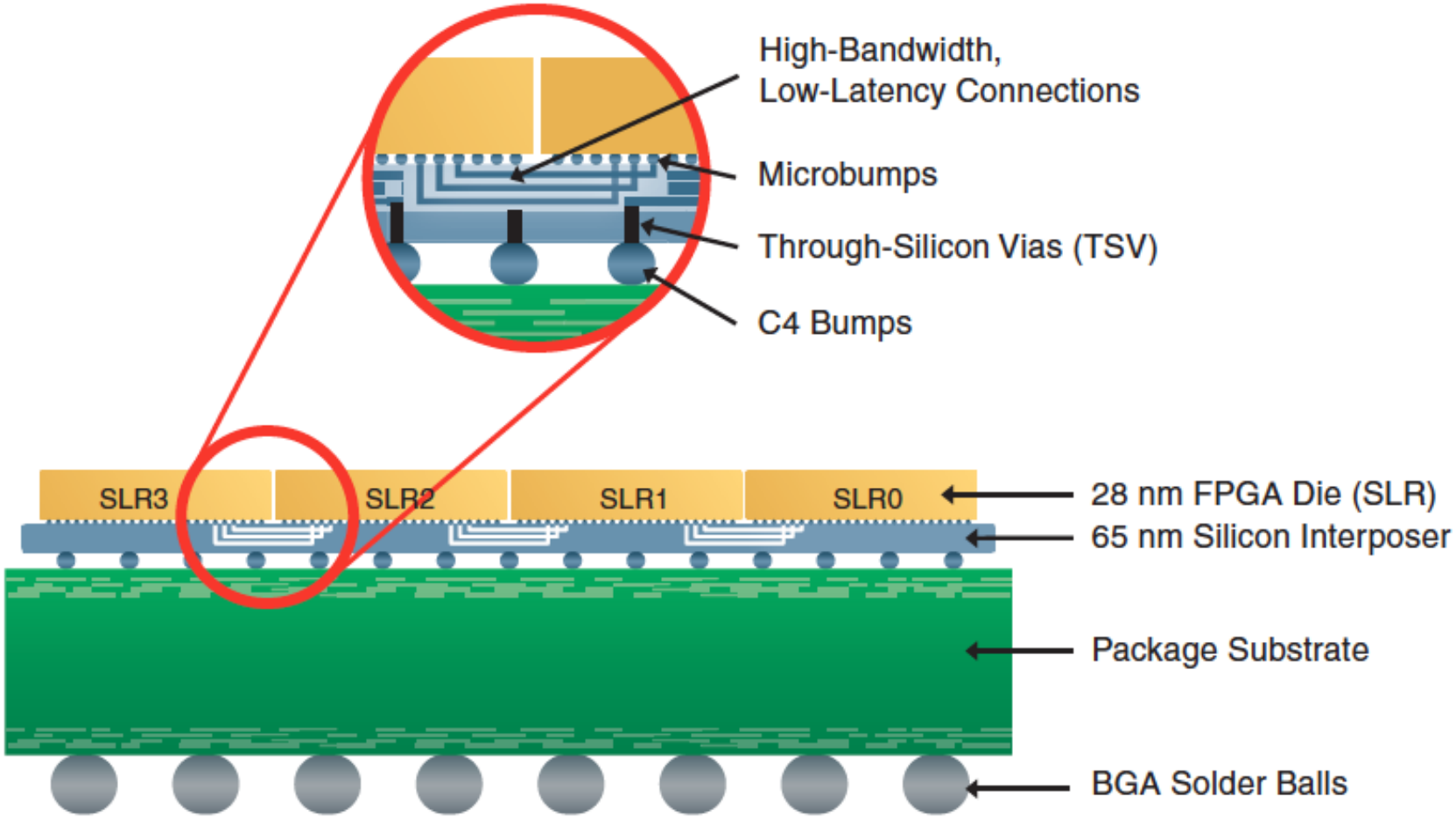
Figure 3: **FPGA SLR (Die) Optimized for SSI Technology**

Interconnection Scheme

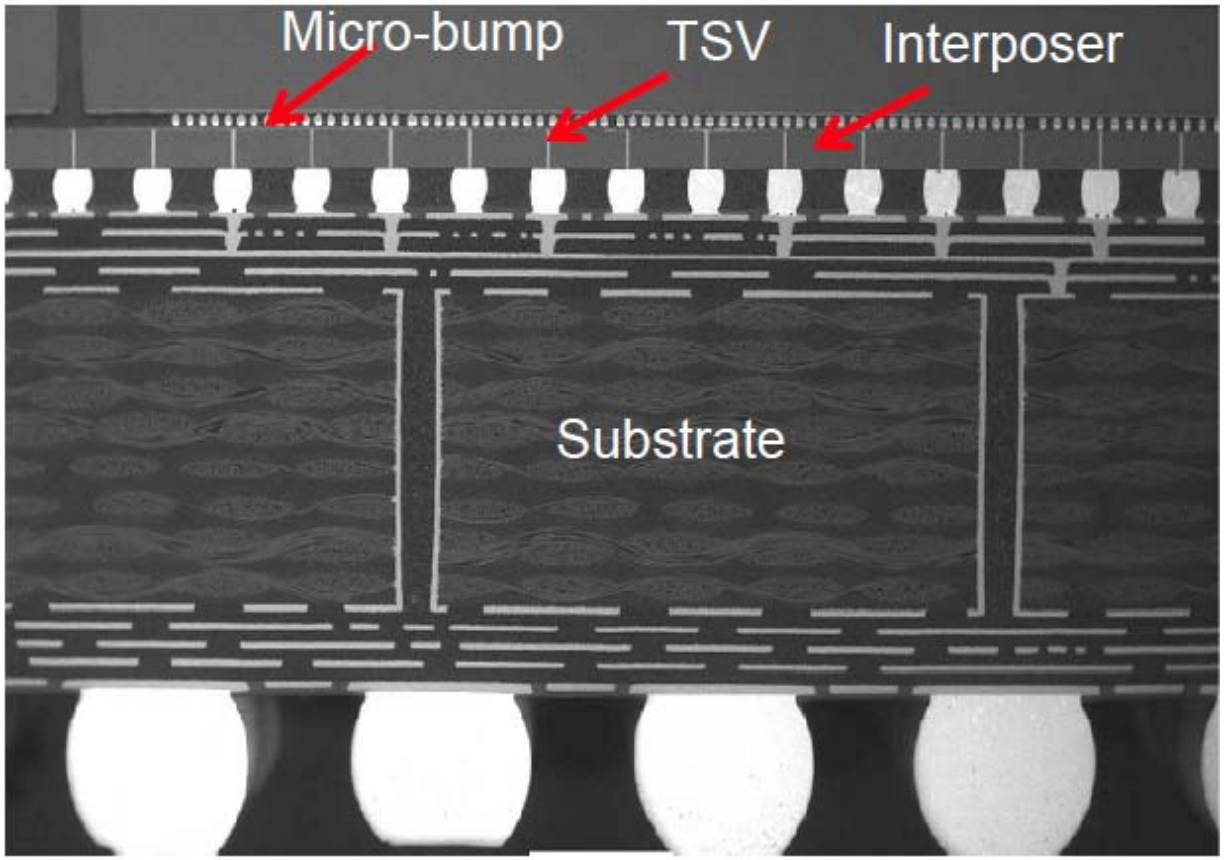
- Each die slice has its own clocking and configuration circuitry.
- The routing architecture has been modified to enable direct connections through the passivation on the surface of the die to routing resources within the FPGA's logic array, bypassing the traditional parallel and serial I/O circuits.
- FPGA Super Logic Region (SLR) is fabricated with microbumps that attach the die to the silicon substrate.
- This enables connections in far greater numbers that reduce latency and overall power consumption when compared to traditional I/Os (100X the SLR-to-SLR connectivity bandwidth per watt versus standard I/Os).



2.5D Package Integration



Stacked Silicon Interconnect Technology (SSIT)
28 nm Active Die with 65 nm Passive Interposer



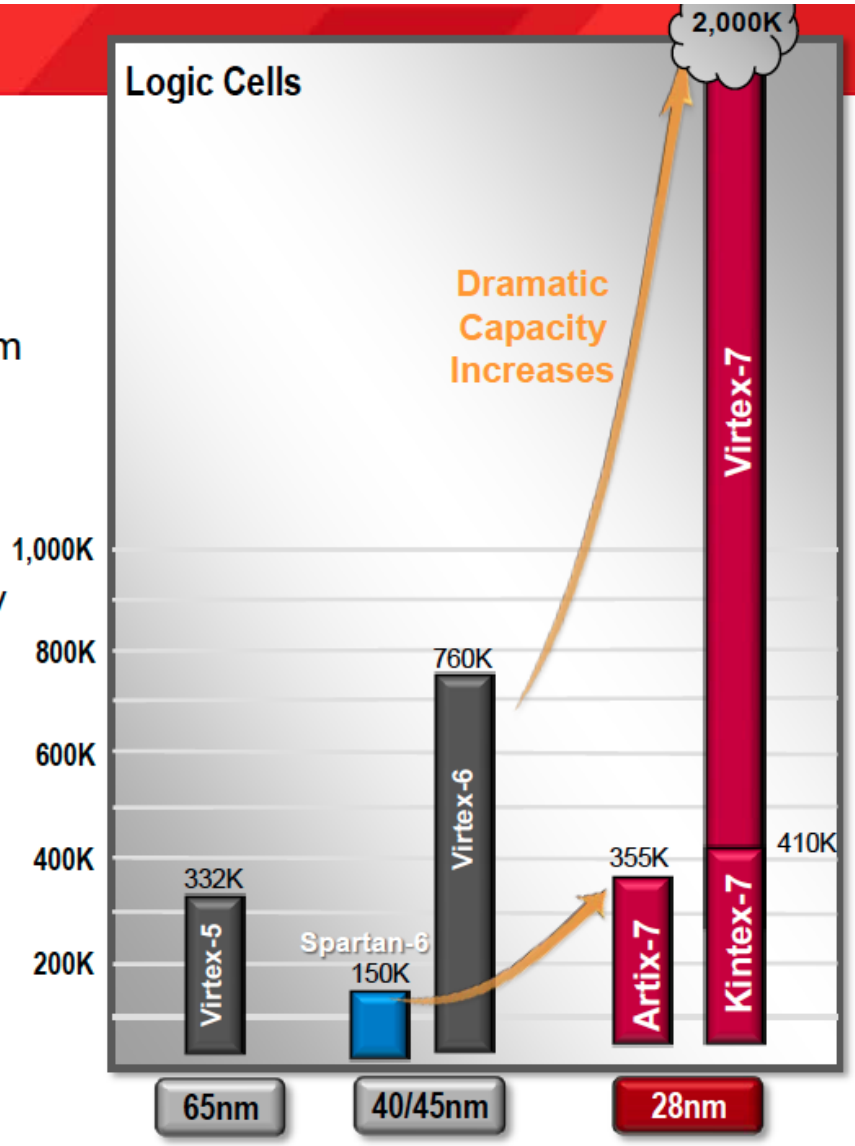
Technology	Specs
M1-M4	2um pitch 4 4X layers
TSV	>10 um diameter & 210um pitch
Micro-bump	45um pitch
C4	210um pitch
Package	4-2-4 Layer, 1.0 mm BGA pitch

- Integrate TSV & μ-bump
- Better FPGA low-k stress management with interposer

Why go to 2.5D Packaging?

- **Challenge:**
  - Frequency scaling is minimal
  - Performance gains focused on parallelism (= capacity)
  - Moore's Law only doubles capacity
- **Solution:**
  - New packaging & assembly methodology
- **Result:**
  > 2x capacity gains over 40nm devices

Family	Capacity Range
Artix-7	20K – 355K LCs
Kintex-7	30K – 410K LCs
Virtex-7	285K – 2,000K LCs



Challenges

- The V7 is a highly optimized part/package that is not specific to the heritage space market – will have to use as is
- Have to use vendor data to qualify
  - Defense grade parts are available now
- Current 28nm HTOL based process reliability = 17 FIT
  - 0.2% to 2% chance of failure at 10 years, 55C to 85C
- 0 fails for 760 DUT w/ 1,000 Cond. B temp cycles (similar FIT rate)
- Radiation performance (alpha & neutron)
  - FIT/MB (memory) & cross section < any other COTS Xilinx products
  - Includes automatic detect and correct circuitry (CRC/ECC)
    - Scans and corrects 2-bit upsets ~30msec
    - CRC/ECC operates independently of user design

Qualification of non-hermetic packages

Table 1-2: **Non-Hermetic Package/Assembly Qualification**

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
THB(1) or HAST(1)	85°C, 85% RH, V_{DD}	1,000 hours	3	25	0 failures
	130°C, 85% RH, V_{DD}	96 hours			
	110°C, 85% RH, V_{DD}	264 hours			
Temperature cycling(1) (2)(3),(4)	–65°C to +150°C	500 cycles,	3	25	0 failures
	–55°C to +125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Autoclave(1) or temperature humidity unbiased(1) or HASTU(1)	121°C, 100% RH	96 hours	3	25	0 failures
	85°C, 85% RH	1,000 hours			
	130°C, 85% RH or 110°C, 85% RH	96 hours or 264 hours			
High-Temperature Storage (HTS)	T_A=150°C	1,000 hours	3	25	0 failures

Notes:

1. Package preconditioning is performed prior to THB, HAST, temperature cycling, autoclave, TH, and HASTU tests.
2. For plastic BGA packages: –55°C to +125°C and 1,000 cycles.
3. For flip chip packages: –55°C to +125°C and 1,000 cycles or –40°C to +125°C and 1,000 cycles.
4. For plastic QFP packages: –65°C to +150°C and 500 cycles or –55°C to +125°C and 1,000 cycles.

Reliability = Knowledge

- More is better
- Require physics of failure
  - Fab
    - TDDB, N/PBTI, EM, etc.
    - What was the definition of failure/test conditions?
  - Package
    - Materials analysis/DPA
- We have to tie our applications to these failure mechanisms
  - Temperature and voltage and radiation and time

System vs. Part

- System reliability becomes the metric of success/reliability
  - Our testing has to connect/mimic application
  - Bit error and/or timing failures
  - NASA/JPL specific BIST for monitoring?
  - FMEA, Weibull, simulation…?
  - Is HALT/HASS beneficial?
- How to tie in design process to reliability
  - Resource utilization

First Steps

- Understand reference designs sensitivity on temperature and voltage and time
  - Are they stable?
  - What is the window of performance?
- Explore system reliability:
  - CAE Tools
  - Weibull models for screening
  - HASS/HALT options
- Do DPA analysis